

# Uday Kumar Reddy B

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Name as it appears on all publications: Uday Bondhugula

## Research Interests

Compilers and runtimes for multicores and other parallel architectures, Automatic parallelization, Polyhedral model, Loop nest optimization, Domain-specific languages, High-performance computing Parallel programming

## Education

- Ph.D. in Computer Science and Engineering Sep 2004 – Aug 2008  
The Ohio State University (OSU)  
Advisor: Prof. P. Sadayappan  
Columbus, OH, USA
- Bachelor of Technology in Computer Science and Engineering Jul 2000 – Jul 2004  
Indian Institute of Technology (IIT), Madras.  
Chennai, India

## Professional Experience

- Associate Professor Dec 2016 – present  
Department of Computer Science and Automation  
Indian Institute of Science  
Bangalore, India
- Assistant Professor Jan 2011 – Dec 2016  
Department of Computer Science and Automation  
Indian Institute of Science  
Bangalore, India
- Postdoctoral Research Scientist Oct 2008 – Dec 2010  
Advanced Compiler Technologies  
IBM T.J. Watson Research Center, Yorktown Heights, New York  
Yorktown Heights, NY, USA
- Visiting Researcher Mar 2008 – May 2008  
ALCHEMY team  
INRIA Saclay (INRIA Futurs), Île-de-France  
Orsay, France
- Research Intern Jun 2007 – Sep 2007  
Advanced Compilation Technologies  
IBM T.J. Watson Research Center, Yorktown Heights, NY  
Yorktown Heights, NY
- Graduate Research Associate Apr'05 – Jun'07, Oct'07 – Aug'08  
Dept of Computer Science and Engineering  
The Ohio State University  
Parallelizing compilers for multi-cores, GPUs  
Columbus, OH, USA
- Graduate Teaching Associate Sep 2004 – Mar 2005  
Dept of Computer Science and Engineering, OSU.  
Instructor – CSE 459.21 Programming in C, CSE 459.23 Programming in Java.  
Columbus, OH, USA

- Summer Intern  
Trilogy Software Inc.

Jun 2003 – Aug 2003  
Bangalore, India

## Publications

1. Diamond Tiling: Tiling Techniques to Maximize Parallelism for Stencil Computations Uday Bondhugula, Vinayaka Bandishti, Irshad Pananilath IEEE Transactions on Parallel and Distributed Systems (TPDS), pgs 1285–1298, vol 27, issue 3, May 2017.
2. A DSL Compiler for Accelerating Image Processing Pipelines on FPGAs  
Nitin Chugh, Vinay Vasista, Suresh Purini, Uday Bondhugula  
IEEE International conference on Parallel Architectures and Compilation Techniques (PACT 2016), Sep 2016.
3. Compiling Affine Loop Nests for a Dynamic Scheduling Runtime on Shared and Distributed Memory  
Roshan Dathathri, Ravi Teja Mullapudi, Uday Bondhugula  
ACM Transactions on Parallel Computing, volume 3, issue 2, Jul 2016.
4. SMO: An Integrated Approach to Intra-Array and Inter-Array Storage Optimization  
Somashakaracharya Bhaskaracharya, Uday Bondhugula, Albert Cohen  
ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL), Jan 2016.
5. The Pluto+ Algorithm: A Practical Approach for Parallelization and Locality Optimization of Affine Loop Nests  
Uday Bondhugula, Aravind Acharya, Albert Cohen  
ACM Transactions on Programming Languages and Systems, volume 38, issue 3, Apr 2016.
6. Automatic Storage Optimization for Arrays  
Somashakaracharya Bhaskaracharya, Uday Bondhugula, Albert Cohen  
ACM Transactions on Programming Languages and Systems (TOPLAS), volume 38, issue 3, Apr 2016.
7. An Optimizing Code Generator for a Class of Lattice-Boltzmann Computations  
Irshad Pananilath, Aravind Acharya, Vinay Vasista, Uday Bondhugula  
ACM Transactions on Architecture and Code Optimization (TACO), Volume 12 Issue 2, Article No. 14, Jul 2015.
8. PolyMage: Automatic Optimization for Image Processing Pipelines  
Ravi Teja Mullapudi, Vinay Vasista, Uday Bondhugula  
International Conference on Architecture Support for Programming Languages and Operating Systems (ASPLOS 2015), Mar 2015.
9. PLUTO+: Near-Complete Modeling of Affine Transformations for Parallelism and Locality  
Aravind Acharya, Uday Bondhugula  
ACM SIGPLAN PPOPP 2015, Feb 2015.
10. Tiling and Optimizing Time-Iterated Computations over Periodic Domains  
Uday Bondhugula, Vinayaka Bandishti, Albert Cohen, Guillain Potron, Nicolas Vasilache  
IEEE International conference on Parallel Architectures and Compilation Techniques (PACT 2014), Aug 2014.  
Nominated for the best paper award.
11. Effective Automatic Computation Placement and Data allocation for Parallelization of Regular Programs  
Chandan Reddy, Uday Bondhugula  
ACM International Conference on Supercomputing (ICS), Jun 2014, Munich, Germany.
12. Automatic Data Allocation and Buffer Management for Multi-GPU Machines  
Thejas Ramashekar, Uday Bondhugula  
ACM Transactions on Architecture and Code Optimization (accepted Nov 2013), selected for presentation at HiPEAC '14, Jan 2014, Vienna, Austria.

13. Compiling Affine Loop Nests for Distributed-Memory Parallel Architectures  
Uday Bondhugula  
ACM/IEEE Supercomputing (SC '13), Nov 2013.
14. Generating Efficient Data Movement Code for Heterogeneous Architectures with Distributed-Memory  
Roshan Dathathri, Chandan Reddy, Thejas Ramashekar, Uday Bondhugula  
International conference on Parallel Architectures and Compilation Techniques (PACT 2013), Sep 2013.
15. PolyGLoT: A Polyhedral Loop Transformation Framework for a Graphical Dataflow Language  
Somashekaracharya Bhaskaracharya, Uday Bondhugula  
International conference on Compiler Construction (CC 2013), Mar 2013, Rome, Italy.
16. Tiling Stencil Computations to Maximize Parallelism  
Vinayak Bandishti, Irshad Pananilath, and Uday Bondhugula  
ACM/IEEE Supercomputing, Nov 2012, Utah, USA.
17. Loop Transformations: Convexity, Pruning, and Optimization  
Louis-Noel Pouchet, Uday Bondhugula, Cedric Bastoul, Albert Cohen, J Ramanujam, P Sadayappan, and Nicolas Vasilache  
ACM SIGACT-SIGPLAN Symposium on Principles of Programming Languages (PoPL), 2011.
18. Combined Iterative and Model-driven Optimization in an Automatic Parallelization Framework  
Louis-Noel Pouchet, Uday Bondhugula, Cedric Bastoul, Albert Cohen, J Ramanujam, P Sadayappan  
Supercomputing (SC) 2010.
19. A Model for Fusion and Code Motion in an Integrated Auto-Parallelizing Compiler  
Uday Bondhugula, Oktay Gunluk, Sanjeeb Dash, and L. Renganarayana  
International Conference on Parallel Architectures and Compilation Techniques (PACT), Sep 2010, Vienna, Austria.
20. Compact multi-dimensional kernel extraction for register tiling  
L. Renganarayana, Uday Bondhugula, Salem Derisavi, Alexandre E. Eichenberger, and Kevin O'Brien  
Supercomputing 2009
21. Compiler-Assisted Dynamic Scheduling for Effective Parallelization of Loop Nests on Multicore Processors  
M. Baskaran, N. Vydyanathan, Uday Bondhugula, J. Ramanujam, A. Rountev, and P. Sadayappan.  
ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP'09), Feb 2009, Raleigh, North Carolina.
22. Data Layout Transformation for Enhancing Locality on NUCA Chip Multiprocessors  
Qingda Lu, Christophe Alias, Uday Bondhugula, Thomas Henretty, Sriram Krishnamoorthy, J. Ramanujam, Atanas Rountev, P. Sadayappan, Yongjian Chen, Haibo Lin, and Tin-fook Ngai.  
International Conference on Parallel Architectures and Compilation Techniques (PACT), 2009
23. A Practical Automatic Polyhedral Parallelizer and Locality Optimizer  
Uday Bondhugula, A. Hartono, J. Ramanujam, and P. Sadayappan.  
ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI '08), Jun 2008, Tucson, Arizona.
24. Automatic Transformations for Communication-Minimized Parallelization and Locality Optimization in the Polyhedral Model  
Uday Bondhugula, M. Baskaran, S. Krishnamoorthy, J. Ramanujam, A. Rountev, and P. Sadayappan.  
International Conference on Compiler Construction (ETAPS CC'08), Apr 2008, Budapest, Hungary.

25. A compiler framework for optimization of affine loop nests for GPGPUs  
M. Baskaran, Uday Bondhugula, S. Krishnamoorthy, J. Ramanujam, A. Rountev, and P. Sadayappan.  
ACM International Conference on Supercomputing (ICS'08), Jun 2008, Kos, Greece.
26. Automatic data movement and computation mapping for multi-level parallel architectures with explicitly managed memories  
M. Baskaran, Uday Bondhugula, S. Krishnamoorthy, J. Ramanujam, A. Rountev, and P. Sadayappan.  
ACM SIGPLAN PPOPP'08, Feb 2008, Salt Lake City, Utah.
27. Automatic mapping of nested loops to FPGAs  
Uday Bondhugula, J. Ramanujam, and P. Sadayappan.  
ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPOPP '07), Mar 2007, San Jose, California.
28. Effective automatic parallelization of stencil computations  
S. Krishnamoorthy, M. Baskaran, Uday Bondhugula, J. Ramanujam, A. Rountev, and P. Sadayappan.  
ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI '07), Jun 2007, San Diego, California.
29. Hardware/software integration for FPGA-based all-pairs shortest-paths  
Uday Bondhugula, A. Devulapalli, J. Dinan, J. Fernando, P. Wyckoff, E. Stahlberg, and P. Sadayappan.  
IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM '06), Apr 2006, Napa Valley, California.
30. Parallel FPGA-based all-pairs shortest-paths in a directed graph  
Uday Bondhugula, Ananth Devulapalli, Joseph Fernando, Pete Wyckoff, and P. Sadayappan  
20<sup>th</sup> IEEE International Parallel and Distributed Processing Symposium (IPDPS '06), Apr 2006, Rhodes, Greece.
31. High performance RDMA-based all-to-all broadcast for InfiniBand clusters  
S. Sur, Uday Bondhugula, A. Mamidala, H.-W. Jin, and D. K. Panda  
12<sup>th</sup> IEEE International Conference on High Performance Computing (HiPC '05), Dec 2005.

## Software and Tools

- Pluto

<http://pluto-compiler.sourceforge.net>

Pluto is a source-to-source parallelization and optimization tool based on the polyhedral compiler framework. It can automatically optimize affine loop nests (sequences of imperfectly nested loops with regular data access patterns) for parallelism and locality using affine transformations. It can target both shared-memory multicore architectures (by generating code with OpenMP parallel pragmas) and distributed-memory architectures (by generating message passing MPI code). Pluto/Pluto+ is extensively used for advanced experimentation with loop optimization and parallelization, optimization of scientific stencil computations, and in university courses teaching loop transformations.

- PolyMage

<http://mcl.csa.iisc.ernet.in/polymage.html>

PolyMage is a domain-specific language and compiler for automatic parallelization and optimization of image processing pipelines. PolyMage takes an image processing pipeline expressed by the user in a high-level language (embedded in Python) and generates a C++ implementation of the pipeline optimized using the polyhedral framework as the intermediate representation. It uses OpenCV for image I/O handling, islpy/ISL for integer set operations, 'cgen' for AST code generation and 'OpenMP' to mark parallel loops. PolyMage uses an asymmetric overlapped tiling technique (overlapped tiling

extended for heterogeneous accesses and non-constant dependence vectors) to exploit locality and parallelism simultaneously. It uses a model-driven approach to automatically fuse image processing pipeline stages for tiling, and employs an in-built autotuner to find the best performing code within a small well-defined search space.

## Research Grants

- Google Faculty Research award (2015)
- AMD research gift in support of research in the area of compilation for heterogeneous multicores (2011–)
- Gift from National Instruments in support of research on compiler optimizations for LabVIEW (2013–2015)
- INRIA Associate Team award (2012–2015) with Albert Cohen (INRIA / ENS)
- NVIDIA GPU research center award for 2012–2013, 2015–2016
- Research grants from Intel labs, Bangalore (2013–2014) and from C-DAC, Bangalore (2013–2014)

## Awards and Honors

- ACM SIGPLAN PLDI Distinguished Reviewer Award as PC member of PLDI 2017
- Indian National Science Academy Medal for Young Scientists 2017
- Indian National Academy of Engineering Young Engineer Award 2016
- Awarded Indian Academy of Sciences Young Associate 2016–2019
- Google Faculty Research Award 2015
- Nominated for the best paper award at PACT 2014 for ‘Tiling and Optimizing Time-Iterated Computations over Periodic Domains’
- INRIA Associate Team award (2013–2015) from INRIA, France (awarded on a competitive basis worldwide)
- Nominated for the ACM SIGPLAN doctoral dissertation award 2008
- ACM SIGPLAN student travel award for PLDI 2008
- All-India Rank 84 (top 0.06%) at the Indian Institutes of Technology Joint Entrance Examination 2000, out of a total of about 1,27,000 candidates
- Represented state of Andhra Pradesh, India at the Indian National Mathematical Olympiad in 1999
- Pratibha scholarship by the Govt of Andhra Pradesh (2000–2004) for performance at IIT-JEE 2000
- Recipient of the National Talent Search Exam (NTSE) scholarship (India) in 1998

## Miscellaneous

- Program chair: IMPACT 2012
- Program committee member: PLDI 2017, Supercomputing 2016, PPOPP 2016, CC 2016, PPOPP 2012, IMPACT 2011–2016; External review committee: PLDI 2014
- Reviewer: LCPC’06, PPOPP’07, ICS’07, LCPC’07, PACT’09, GPGPU workshop 2010, PPOPP 2011, HPCA 2011, IMPACT 2011–2016, ACM TOPLAS, ACM TACO, IEEE TPDS, JPDC
- Table Tennis: The Ohio State University team (2007 - short while), IISc TT tournament champions 2013 (CSA team)

- Football: IISc university team (2012 - present), IISc university tournament champions 2011-2012, 2012-2013, Bangalore C-division player
- Swimming: Karnataka state masters championships 2013 – 50m freestyle bronze, 4x50m medley relay bronze, 4x50m freestyle relay bronze – NCBS/IISc team
- Languages: English (fluent), Hindi (native), Telugu (native), French (intermediate), Kannada (intermediate)